REMARKS

Examiner Picardat is thanked for his thorough search and Office Action. Reconsideration of the rejection of all claims is respectfully requested. We wish to comment on his remarks as follows:

Examiner's ruling with respect to the restriction of claims is duly noted. Claims 31-36 are hereby canceled. A divisional application will be filed at the appropriate time.

Reconsideration is requested of all rejections based on 35 U.S.C. 103:

The present invention teaches a method for packaging a semiconductor wafer by covering it with a polymeric layer and then forming conductive posts that pass through said layer to contacts at the wafer surface. The invention further teaches the use of plating (both electro and electroless) for forming the posts and then addresses several alternative ways to accomplish this. The invention also provides guidelines as to some of the physical properties that the posts must have in order to operate reliably.

Examiner Picardat has cited three references which, it is claimed, could be combined to generate the present invention. These are:

Kata et al. which teaches covering a wafer with a polymeric layer and then forming posts within the layer which connect to contact pads at the wafer surface. More specifically, they teach use of a carrier film bearing a redistribution network which they bond to the wafer. Said redistribution network is for I/O within a chip, not between chips. We have already stated in our application (page 7 lines 7-8) that such redistribution networks are standard.

Malloy et al. teach running connections between an internal terminal point on the surface of an integrated circuit to an external contact on the package surface . This is an aspect of any standard redistribution network.

Farnsworth teaches an improved process for forming a UBM (under ball metallurgy) pad for a flip chip. Examiner has asserted that Farnsworth "discloses the metal layer to extend into the dicing area to connect the chips while in wafer form". Absent any indication from Examiner as to where in Farnsworth this information is located, we have read through this reference several times without finding it. We therefore believe that Examiner is mistaken in his assertion. If not, could he please provide us with a column/line reference so that we may find it.

We would also respectfully draw Examiner's attention to the following novel features of the present invention against which no prior art references have been cited:

In claim 1, our teaching that the material from which the posts are formed must be able to bend in order to absorb stress.

In claims 4, 13, and 24, our teaching that laser drilling may be used to form the via holes that will house the posts.

In claim 5 and 19, our teaching that the posts may be formed through electroless plating.

In claim 6, our teaching that the material from which the posts are to be formed must behave according to the disclosed formula.

In claim 8, our teaching that electroforming of the posts can be achieved by connecting through a temporary common distribution network comprising the chip-level redistribution networks connected to each other in the kerf and, after posts are formed, slicing the wafer into individual chips, thereby cutting all lines in the kerf area and electrically dividing said common distribution network into chip-level redistribution networks.

In claim 11, our teaching that a photo sensitive version of the polymeric material may be used to form the via holes.

In claims 15, 22, and 25, our teaching that said photosensitive polymer layer be used to

provide a negative image of the mask, thereby causing the via holes to be wider closest to the second layer of metal (and thus more robust).

In claims 16 and 26, our teaching that said photosensitive polymer layer may be used to provide a positive image of the mask, whereby, through use of an imaging system having a low depth of focus and focusing in a plane midway into the via hole, the via holes are shaped so as to be narrowest at a point halfway down the holes (thereby making the posts more robust).

In claim 17, our teaching that a lollipop structure may be formed from the post and solder bump combination.

In claim 29, our teaching that the solder bumps may be laid down using screen printing or stenciling.

In claim 30, our teaching that electroplating within the via holes can be accomplished by depositing a contacting layer of metal over the passivating layer, coating this with photoresist within which the via holes are formed, and then forming the posts by means of electroplating. Then removing the photoresist thereby forming freestanding metal posts. Then, without attacking the posts, removing the contacting metal layer and spreading over the entire wafer a layer of polymeric material while leaving part of the posts uncovered;

In conclusion, we again thank Examiner Picardat for his careful reading of our application.

Reconsideration and withdrawal of the rejection is respectfully requested.

Allowance of all Claims is requested. It is also requested that should Examiner Picardat not find that the Claims are now Allowable, he should please call the undersigned Attorney at (914)-452-5863 to overcome any problems preventing Allowance.

Respectfully submitted

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